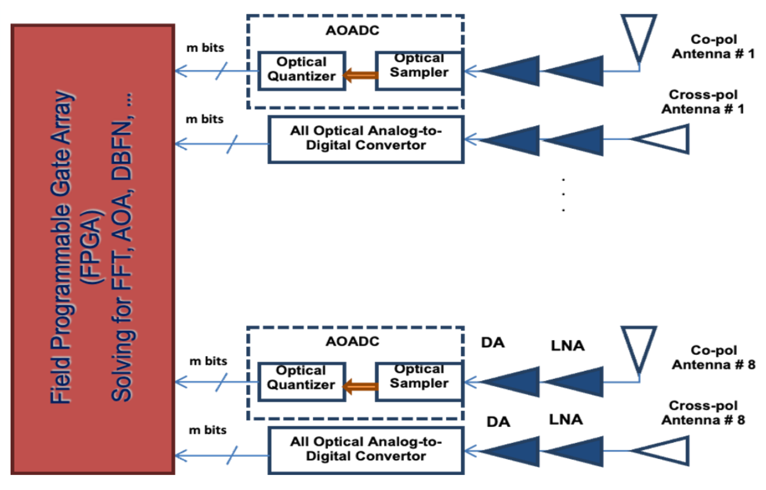
Millimeter-Wave Dual-Mode RF Front-End Circuits for All-Optical ADC

Group 37: L. Daukaus, J. Cargill, and A. Hoyt| **Advisors:** Prof. Ashin S. Daryoush and PhD Candidate Joseph Fasbinder

Introduction

- Future generations of radar, remote sensing, wireless communications, and surveillance technologies are reliant upon high frequency broadband digital receiver chips capable of capturing millimeter wave signals and digitize at rates of 40GSPS with 10 effective bits that requires high dynamic range and low power consumption of under 1W
- All optical ADC (AOADC) using optical clock sampling and optical quantizer is a novel low power consuming solution on silicon photonics.

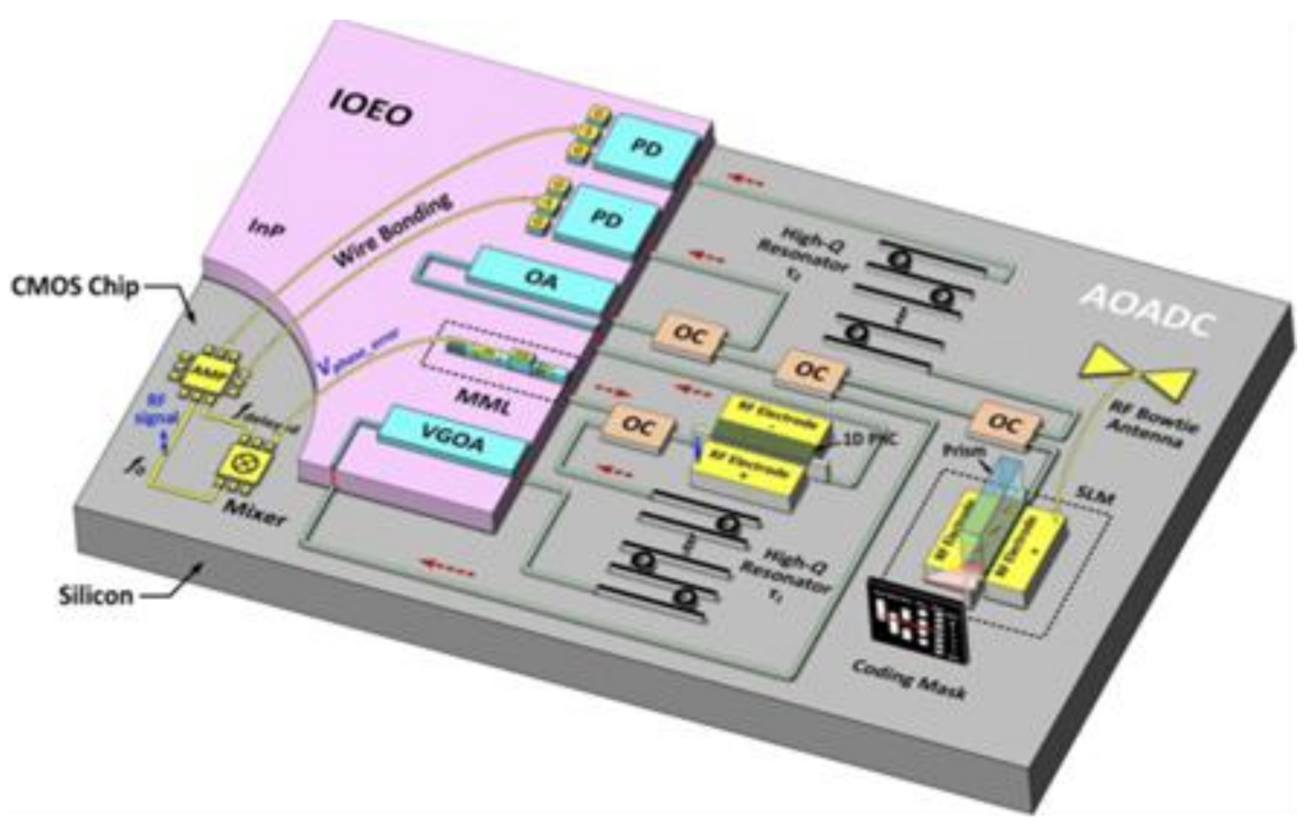
Challenge of global connectivity of airborne/spaceborne flyers in support of Naval operations



Dual Polarized Phased Array Antennas with Direct Digital Receivers using AOADC

Background

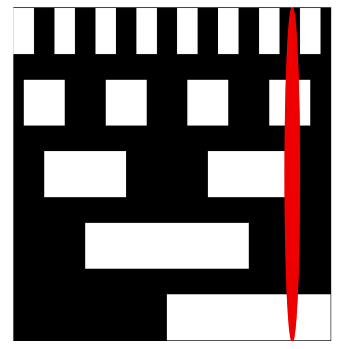
- Novel 40 GSPS AOADC with 10 ENOB and <1W power outperforms multiple time interleaved-ADCs with >4W power consumption.
- RF signals of 20-40GHz require flat gain and good matching across a wide range of frequencies.
- The front-end must provide high gain while keeping noise and distortion low to preserve usable range.
- Mixing and amplification stages must remain stable, isolated, and power-efficient to ensure reliable system operation.
- SiGe-BiCMOS is amenable to mixed signal integrated circuit realization on Si platform by developing custom amplifiers.



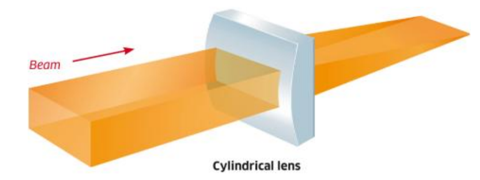
- An RFIC integrates the complete high frequency signal chain including amplification, mixing, oscillation, and impedance control onto a single millimeter wave chip.
- An AOADC RFIC integrates a millimeter wave radio frequency front end with an optical quantization interface on a single chip to enable high speed digitization with reduced electrical jitter, lower power consumption, smaller system size, and improved dynamic range.

Optical Quantizer Experiment

- Quantization circuits using leaky waveguide technology with spatial light modulator received by a photodiode array will have quantization error
- Experiment designed to quantify error replicating optical quantizer of RFIC using CCD camera as photo collector and laser pointer as optical source with lens to narrow beamwidth for binary / gray code mask



5 Bit Mask



Cylindrical Lens Operation

$$\frac{1}{s}+\frac{1}{s'}=\frac{1}{f} \qquad M=\frac{h'}{h}=-\frac{s'}{s}$$

Dimensions For Different Setups

Number of Bits	Number of Quantizers	Minimum Width (um)	Minimum Length (um)	Source Location (cm)	Focal Length (mm)
4	3	132	346	61	19.4
5	2	99	376	81	19.5

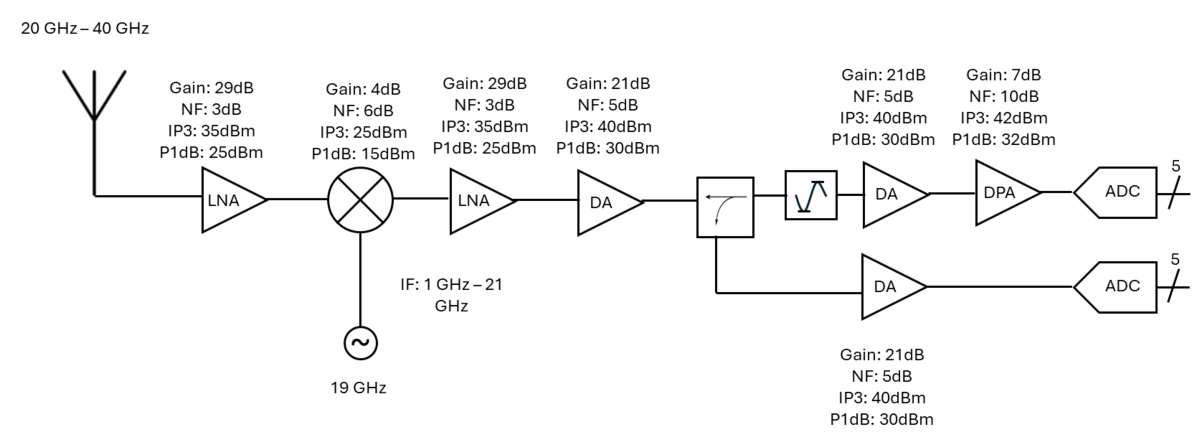
Dimensions of CCD Array

	Pixel count	Pixel size	Total size
Vertical	1360	4.65um	6.324mm
Horizontal	1024	4.65um	4.762mm

- Dimensions calculated using the lens equations, as well as considering CCD size and number of positions to consider
- Each slit needs to be printed using transparency paper, with slit size and printing capabilities limiting factor for number of bits able to be tested

System Level Analysis

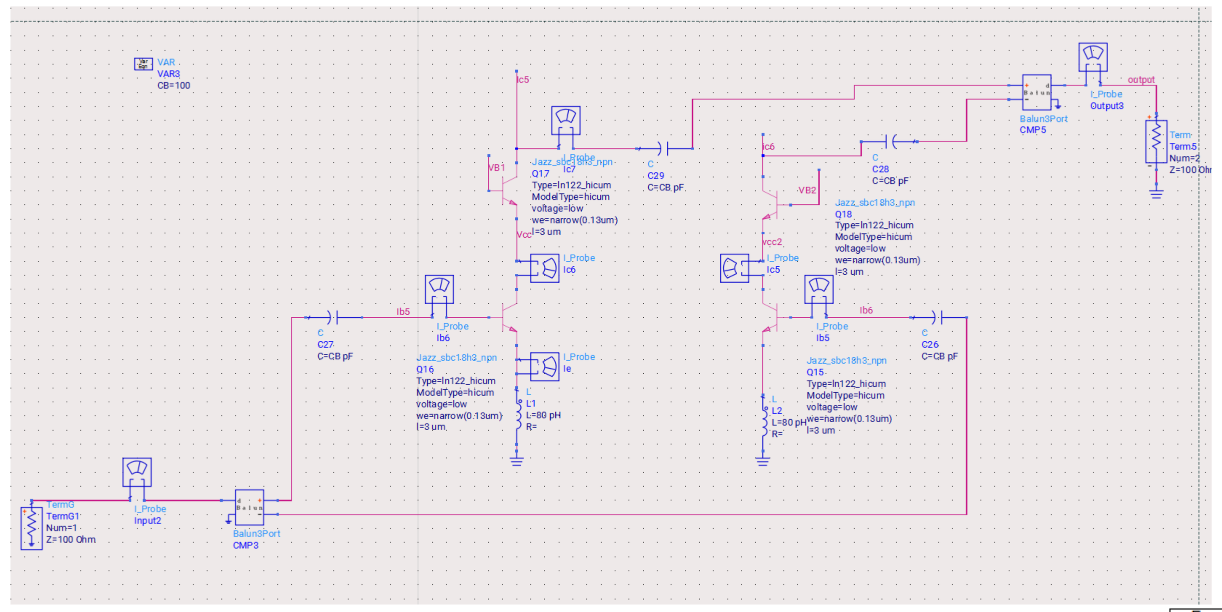
- System performance critical for achieving 10ENOB at ADC
- Design considers both noise and harmonic distortion as main reduction in ENOB for AOADC
- Focus on two parallel 5 bits as viable solution as opposed previously proposed solution of three 4 bits

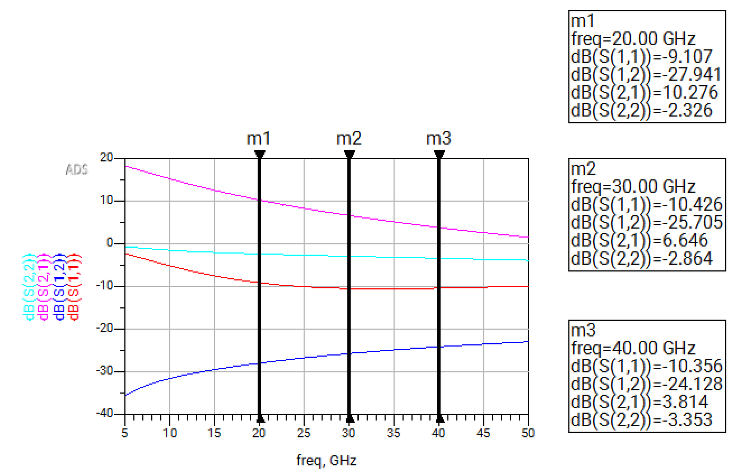


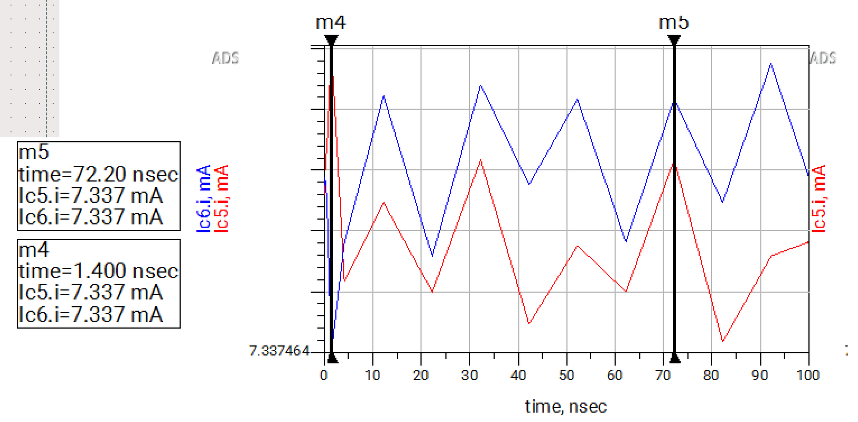
Proposed Configuration

Modeling of RF Driver from Antenna

- Broadband Low Noise Amplifier(20-40GHz) implements a differential cascaded topology with SiGe HBT
- The balanced architecture allows for wideband gain with improved isolation and reduced Miller feedback for better stability/bandwidth

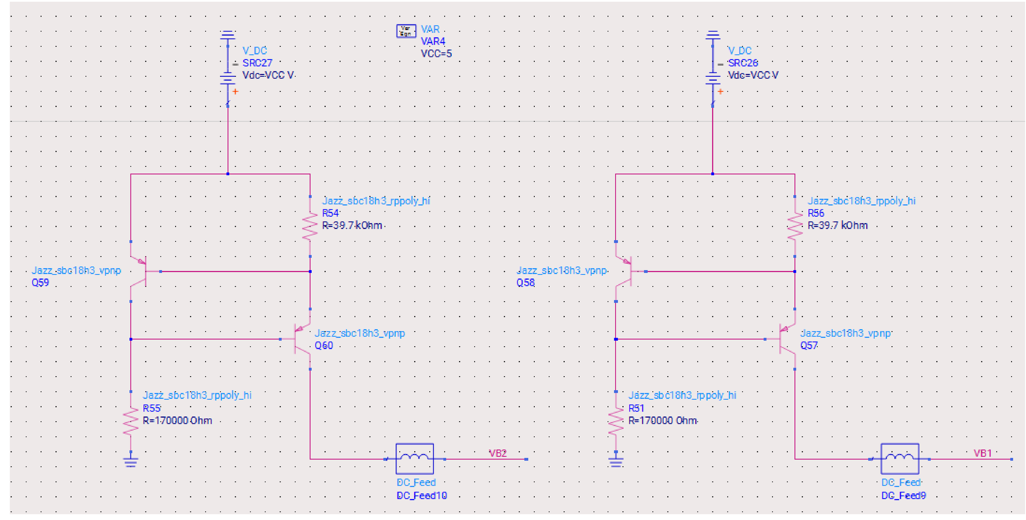


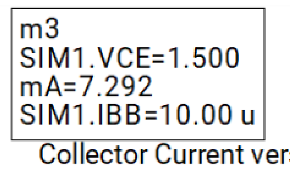




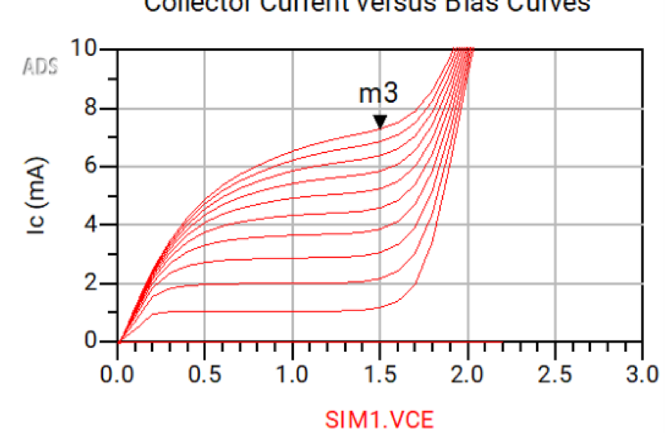
- Graphs
  - S-Parameters for single cell
  - Differential Current Symmetry check

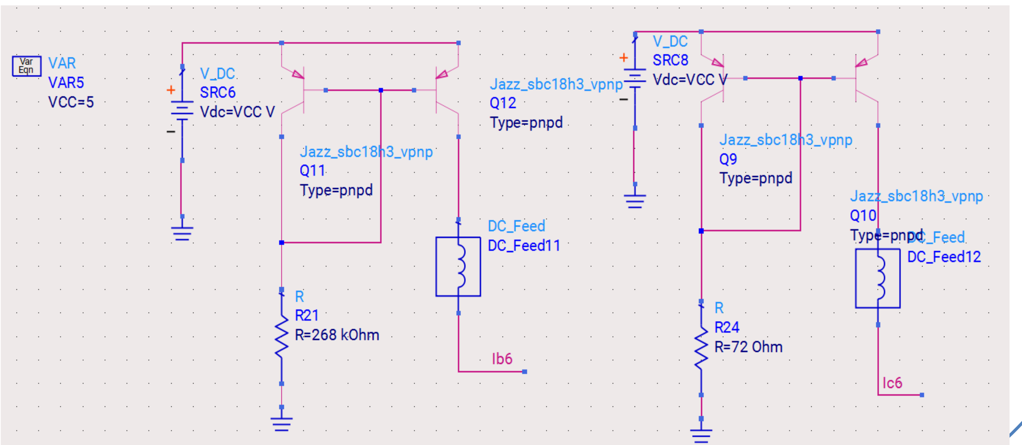
- Class AB Bias operating point was selected at VCE = 1.5 V and IB = 10 microamps this results in approximately IC = 7.292 mA
- VB biases to the cascaded transistors' base
- Ib biases the input transistors' base
- Ic biases the output collector





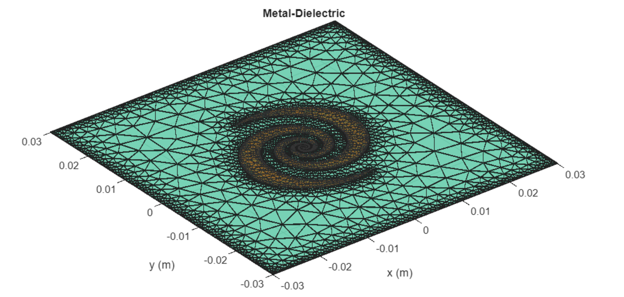
Collector Current versus Bias Curves



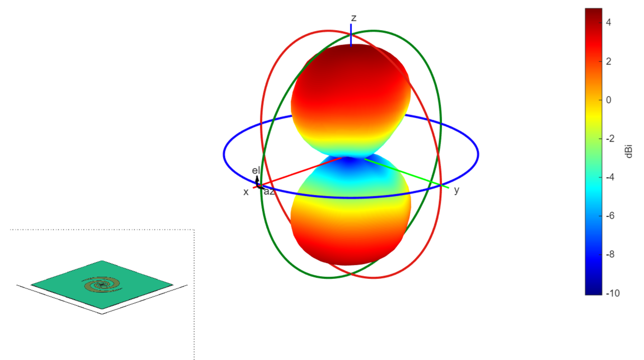


Broadband Spiral Antenna

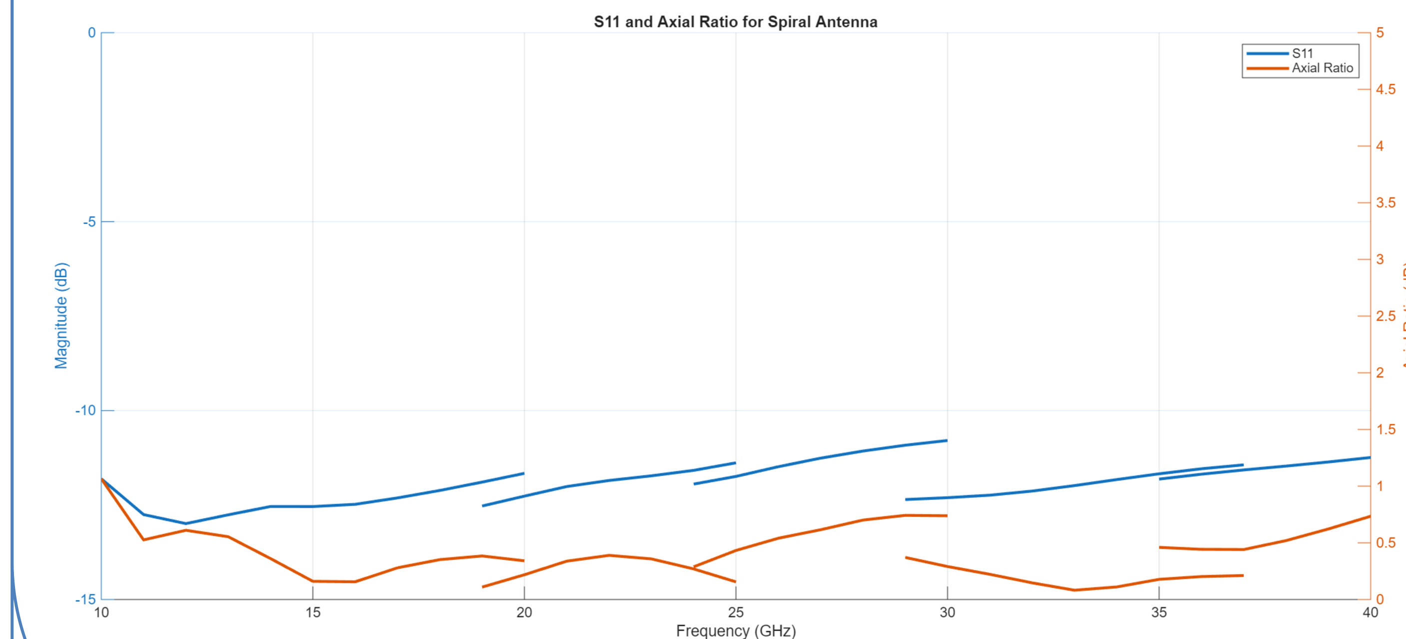
- Antenna from previous SD groups originally tested from 1-21 GHz
- Simulations performed at 21-40 GHz to ensure performance across higher frequency range
- Discontinuities in plots due to batching of simulations with variable meshing
- Results show high efficiency and near ideal polarization across spectrum



Antenna Simulation Meshing



Radiation Pattern



S11 and Axial Ratio Results

Conclusions

- Keysight ADS design modeling for RFIC simulations of Low Noise Amplifier
- Setup experiment for Optical Quantizer
- Antenna simulations and modeling complete

Next Steps:

- Match and stage LNA cells, and complete mixer schematics
- Develop RFIC layout and optimize performance using EM simulator.
- Full system modeling and analysis
- Antenna fabrication and anechoic chamber testing